Remarks

Claims 1, 5, 10, 11, 20, 21, 24 – 28, and 30, inclusive have been amended. Claim 23 has been cancelled. Claims 31 – 37 are withdrawn, inclusive. New claims 38 and 39 have been added.

I. Status of the Application.

Following the above amendments, claims 1 – 22, 24 – 30, and 38 – 39 are pending. Claims 38 – 39 are new, and have been added to further clarify the linearizing circuit architecture of the present invention.

In the February 16, 2006 Office Action (the "Office Action"): (1) the drawings were objected to based upon the "oscillator" of claim 20 (Office Action page 4); (2) claims 1 – 25 and 28 – 30 were rejected based upon various Section 112 informalities, with claims 2, 3, 5, 6, 10 – 12, and 15 – 25 being allowable when rewritten to overcome the Section 112 rejections (Office Action pages 4 – 7); (3) claims 1, 4, 7 – 9, 13, 14, and 28 – 30 were rejected as anticipated under Section 102 based on Dickson U.S. Patent Application Publication No. US 2004/0013348 ("Dickson" or the "Dickson reference") (Office Action pages 6 – 7); and (4) the Examiner requested a written affirmation of elected claims 1 – 30 following a restriction requirement (Office Action pages 2 – 3).

With respect to the restriction requirement, Applicants hereby affirm the prior election of the invention of Group I, claims 1 – 30, and claims 31 – 37 have been withdrawn.

In this response, Applicants have amended claims 1, 5, 10, 11, 20, 21, 24 – 28, and 30, and have added new claims 38 – 39. Applicants respectfully traverse the rejection of claims 1 – 25 and 28 – 30 under Sections 112 and 102. Applicants respectfully request reconsideration of the pending claims in view of the foregoing amendments and the following remarks.

II. The Objection to the Drawings and the Rejection of Various Claims Under Section 112 Should Be Withdrawn.

(A) With respect to the objection to the drawings, the Examiner is directed to Figure 2, which is a circuit diagram illustrating a voltage controlled oscillator having reference numeral 150. In addition, the Examiner is directed to paragraphs 39, 41, 57, 69 and 70 of the published Specification, discussing the use of an input voltage or an applied voltage to control the frequency of the oscillator 150 and the capacitance of its incorporated capacitor (junction varactor). Accordingly, the objection to the drawings should be withdrawn, as the oscillator is illustrated in Figure 2.

(B) With respect to the objection to claim 30 under section 112, first paragraph (Office Action page 5), the Examiner is directed to Figure 9 and to paragraph 66 of the Specification, which demonstrate that the step of determining a logarithm (step 540) is not critical to or essential to the practice of the invention. Rather, either a logarithm (step 540) or a 3/2 power function (step 530) is utilized, depending upon the degree of approximation selected (in step 525). This is also explicit in paragraph 66, describing the use of the logarithm as an approximation to the 3/2 power function and its implementation with weak inversion CMOS electronics. Accordingly, the objection to claim 30 should be withdrawn.

(C) With respect to the objection to claim 1 and claim 21 (and their corresponding dependent claims 2 – 20 and 22 – 25) under section 112, second paragraph (Office Action pages 5 – 6), concerning how the logarithm generator is adapted to generate an applied signal which is substantially proportional to the sum of the square root signal and a logarithm of the input signal, the Examiner is directed to paragraphs 77 – 81 of the Specification. In one embodiment, the logarithm generator is implemented as a transistor (M4 of logarithm generator 330 in Figure 6) operating in weak inversion and forward saturation of the drain current, which provides an output signal which is substantially proportional to the logarithm of the input signal (Equation 23) and which is added to the square root voltage (level shifted as the V_{GS} (gate to source voltage) from node 320) (paragraph 81). In another

embodiment, a programmable processor (such as a digital signal processor) implements the square root and logarithm generation functions, including any combining or addition functions (paragraph 91). In another embodiment, a summing function in a combiner 235 is utilized (Figure 5 and paragraph 73). Accordingly, Applicant's respectfully traverse the rejection of claims 1 and 21 under section 112, second paragraph. The objection to claims 1 and 21, and their corresponding dependent claims, should be withdrawn.

In addition, Applicants have amended claims 1 and 21 to include circuitry which comprises the logarithm generator, and which provides an applied signal which is substantially proportional to the sum or the superposition of the square root signal and a logarithm of the input signal. Accordingly, circuitry has been claimed which performs the claimed operations.

(D) Claim 5 has been amended to correct its claim dependency. In addition, claims 10 and 11 have been amended to more clearly specify that the selected parameter, such as a frequency response of an oscillator, varies substantially linearly with the input signal and substantially nonlinearly with the applied signal.

(E) With respect to the objection to claim 20 under section 112, second paragraph (Office Action page 6), concerning an apparent lack of support in the Specification for an "'apparatus to provide a substantially linear relationship between an input signal and a selected parameter' including 'an oscillator'", the Examiner is directed to Figure 2, illustrating a voltage controlled oscillator having reference numeral 150. In addition, the Examiner is directed to paragraphs 39, 41, 57, 69 and 70 of the Specification, discussing the use of an input voltage or an applied voltage to control the frequency of the oscillator 150 and the capacitance of its incorporated capacitor (junction varactor). For example, paragraphs 41 and 69 – 70 describe the pre-processing of the input signal, to form an applied signal, to allow a frequency response of a capacitor or junction varactor 100 within an oscillator 150 (as a selected parameter) to vary linearly with the input signal.

In addition the Specification has been amended to incorporate claim 20 and

provide verbatim support within the Specification. Accordingly, the objection to claim 20 should be withdrawn.

III. The Rejection of Various Claims Under Section 102 Should Be Withdrawn.

The Dickson reference does not disclose and does not suggest the claimed features of the present invention. First, Dickson does not disclose and does not suggest creation of an intermediate, applied signal, which varies substantially nonlinearly with the input signal and further, when applied to a selected parameter such as a frequency response, allows the selected parameter to vary substantially linearly with the input signal, thereby allowing linear control over the parameter. Rather, Dickson creates a direct signal to control a dither amplitude to actuate mirrors for attenuating optical power coupling for data transmission in fiber-optical systems.

Second, Dickson does not disclose and does not suggest, as claimed in the various independent claims 1, 21, 26, 27, 28, 30 and 39, the creation of such an intermediate, applied signal based upon the summation or superposition of a square root signal (proportional to the square root of the magnitude of the input signal) with a logarithmic signal (proportional to the logarithm of the magnitude of the input signal). This claimed feature is patentably distinct from Dickson, which utilizes a summer to form a difference between two logarithms of input and commanded power. A square root function then converts the one resulting logarithm difference into an initial estimate of dither amplitude.

Accordingly, nothing in Dickson discloses or suggests performing a sum or superposition of a square root signal with a logarithm signal to create an intermediate, applied signal, which varies substantially nonlinearly with the input signal. Further, nothing in Dickson discloses or suggests applying such an intermediate signal to control a selected parameter, such as a frequency response, to thereby allow the selected parameter to vary substantially linearly with the input signal.

Dickson further does not disclose or suggest any of the claimed features of the

various other independent and dependent claims, such as claims 2, 3, 5, 6, 10 – 12, and 15 – 25 which the Examiner has found to be allowable.

In addition, use of the circuitry and the equations of Dickson would provide the wrong result if applied to the parameter control of the present invention. Dickson does not create a predistorted signal which, when applied to a selected parameter, allows the parameter to vary linearly with an input signal. Dickson would simply create an attenuation of power. Accordingly, Dickson teaches away from the present invention. Such teaching away is the antithesis of art suggesting that a person of ordinary skill go in the claimed direction. See *In re Fine*, 873 F.2d 1071 (Fed. Cir. 1988). This teaching away from Applicants' invention is a *per se* demonstration of lack of obviousness and a lack of anticipation.

In addition, identification of any individual part claimed is insufficient to defeat patentability of the whole claimed invention. See *In re Kotzab*, 217 F.3d 1365 (Fed. Cir. 2000). Accordingly, no *prima facie* showing of potential anticipation or obviousness has been made, and any assertions to the contrary have been clearly rebutted. *In re Rouffet*, 149 F.3d 1350 (Fed. Cir. 1998); *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990). The rejection of claims 1, 4, 7 – 9, 13, 14, and 28 – 30 as anticipated under Section 102, therefore, should be withdrawn.

In addition, new claims 38 and 39 should therefore be passed to issue along with the other claims remaining in this case. New claim 38, dependent from claim 1, provides for the square root converter and circuitry comprising a logarithmic generator to be embodied as a processor, such as a digital signal processor. New claim 39 is allowed claim 2 rewritten in independent form, as suggested in the Office Action (page 7).

The remaining references also do not disclose or suggest, alone or in combination, the present invention. Takahashi et al. Patent Application Publication US 2006/0012435 provides a current detector having an output modified by an n^{th} root or a logarithmic converter. Nawracala U.S. Patent No. 6,775,002 B2 includes a logarithm amplifier. Gilbert U.S. Patent No. 6,549,057 B1 utilizes a difference of squares function to provide an implicit square-root function. Gilbert U.S. Patent No. 6,429,720 B1 also utilizes a squaring function. Hanna U.S. Patent No.

6,118,879 utilizes a logarithmic function in a BTSC encoder. Hanna U.S. Patent No. 5,796,842 utilizes a squaring function and a square-root function in a BTSC encoder. Morris U.S. Patent No. 5,523,875 utilizes a logarithmic amplifier. D'Angelo et al. U.S. Patent No. 5,473,279 utilizes a square law expander and an inverse square law compressor. Alm U.S. Patent No. 4,712,010 utilizes a nonlinear (logarithmic or square root) gain control. Rice, Jr. U.S. Patent No. 3,712,977 utilizes a square-root circuit. Lastly, Baudino U.S. Patent No. 3,562,552 utilizes a log converter to provide an output signal which is a square root of an input DC mean squared signal.

None of the cited references disclose or suggest the claimed elements of the present invention. The present invention, therefore, is not anticipated and is not rendered obvious by these references under Sections 102 and 103, and the rejection of the claims should be withdrawn. In addition, because the remaining dependent claims incorporate by reference all of the limitations of the corresponding independent claims, all of the dependent claims are also allowable over the cited references.

On the basis of the above amendments and remarks, reconsideration and allowance of the application is believed to be warranted, and an early action toward that end is respectfully solicited. In addition, for any issues or concerns, the Examiner is invited to call the attorney for the applicant at the telephone number provided below.

A check in the amount of $60.00 is enclosed to cover the Petition fee. Please charge any additional fees or credit any overpayments as a result of the filing of this paper to our Deposit Account No. 02-3978.

Respectfully submitted,

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